Radiation Assurance Test in BMTI

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Beijing Microelectronics Technology Institute

EEE Components Radiation Test Workshop

31st March – 1st April, 2016

Outline

- A general BMTI introduction
- Using built-in self-test (BIST) structures for SEE test
- SEE failure analysis with laser
- Test method for distinguishing SEU and SET, and SET analysis

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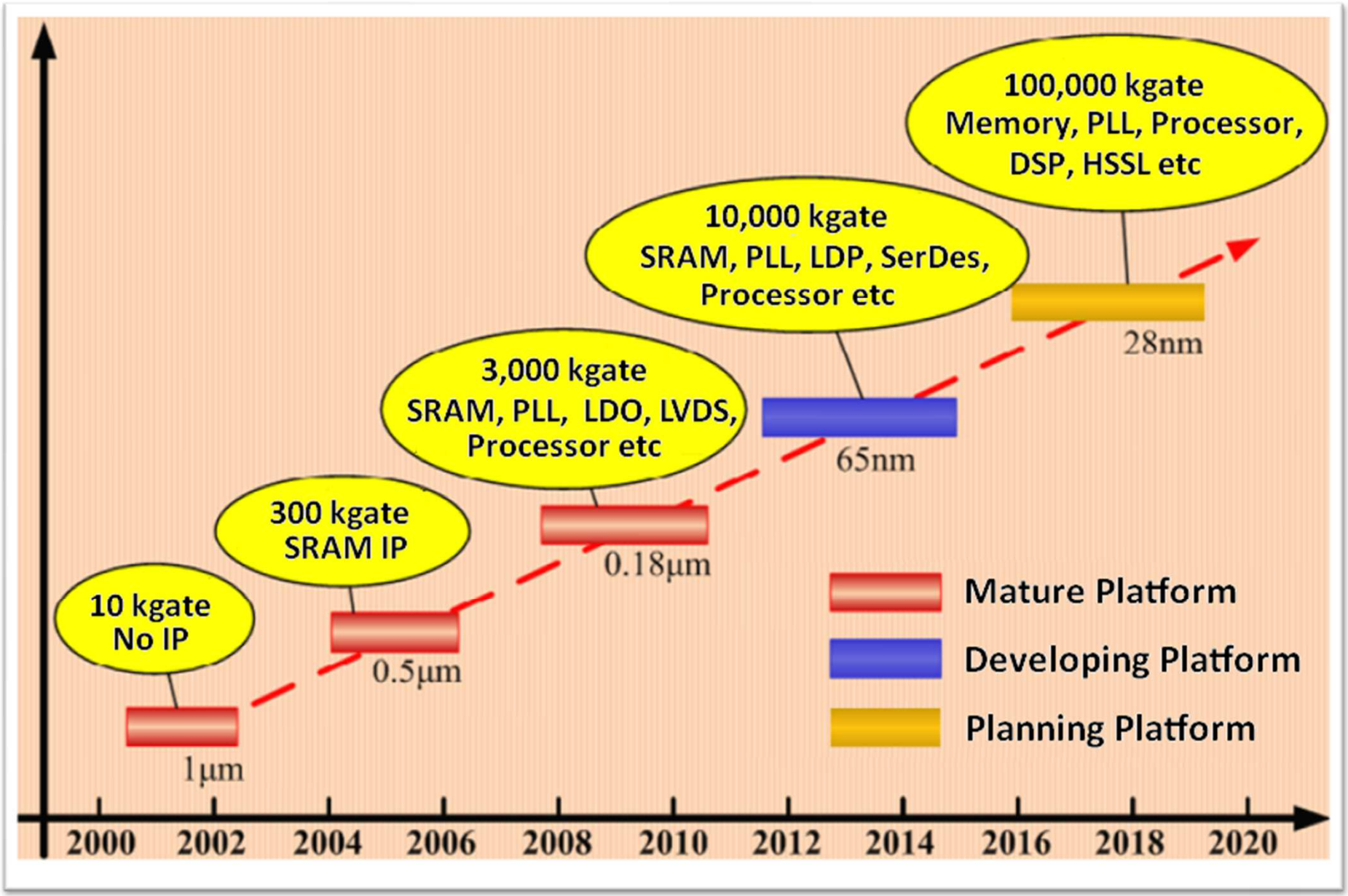
A General BMTI Introduction

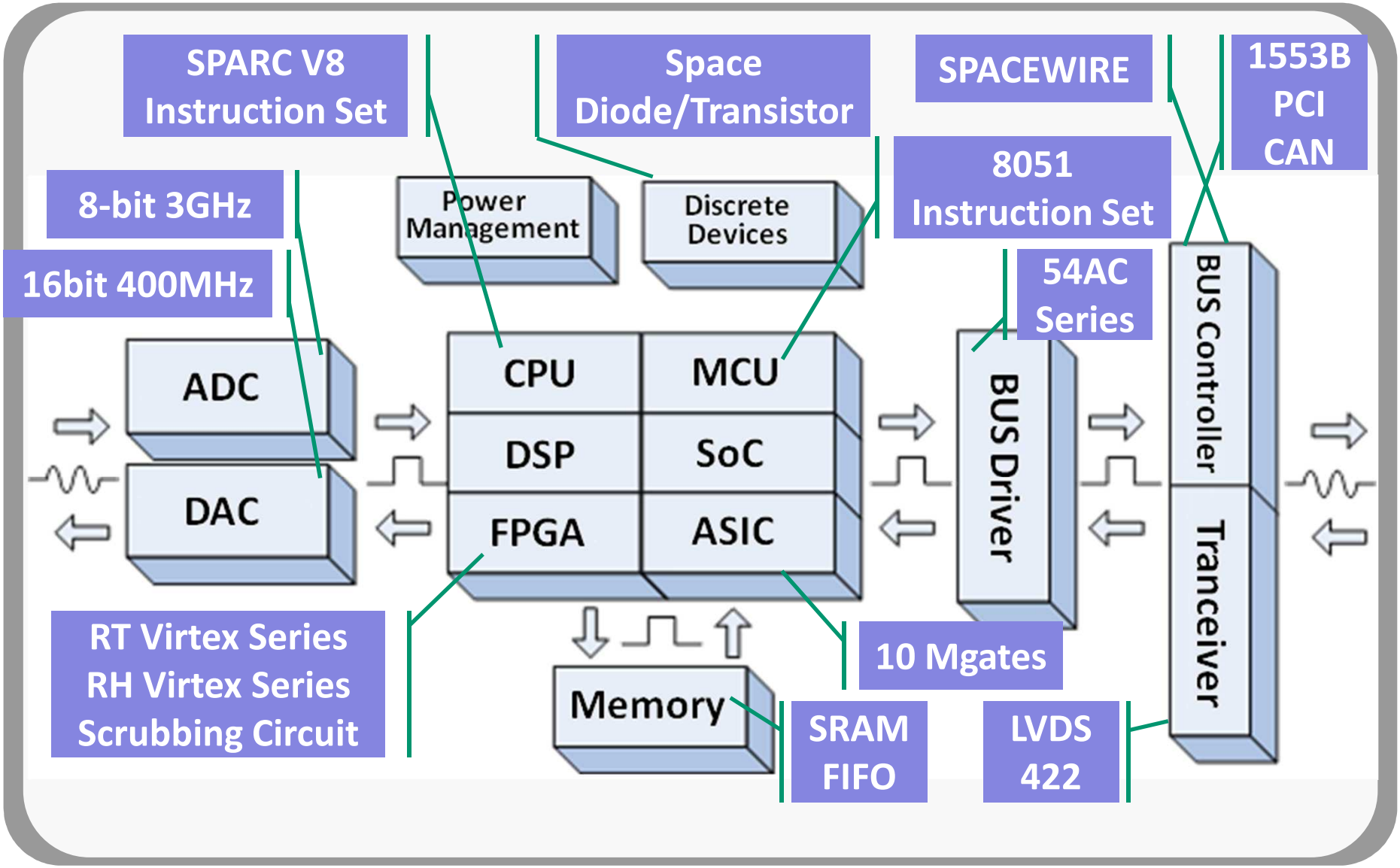
- **BMTI is a China leading organization in radiation-hardened microelectronics research**
- **Also the largest radiation-hardened IC provider in China**

- **The main achievements include:**
  - **Several high-reliability RH IC design platforms**
  - **A complete RH IC product family**
  - **Advanced packaging, testing, and 4-inch fab line**

BMTI's Radiation-Hardening Design Platforms



BMTI's Space IC Product Family



Packaging, Testing and Fab Lines

✓**Ceramic package line**

- **Up to 1,500 pins**
- **BGA/QFP/PGA/LCC/DIP/CCGA**
- **MCM/3-D packaging**

✓**Testing line**

- **Up to 1,024 test channels**
- **Up to 1GHz test frequency**
- **FPGA/SoC/RF/ADC/DAC/Memory chips**

✓**Reliability assessment**

- **Screen and Qualification Inspection**
- **Up to 25MHz Burn-in frequency**
- **Compliant with GJB548 (MIL-STD-883), GJB33 (MIL-PRF-19500)**

✓**0.8μm, 4-inch fab line**

- **Space diode/transistor/VDMOS**
- **MEMS**
- **Capable of processing 3,000 wafers/month**

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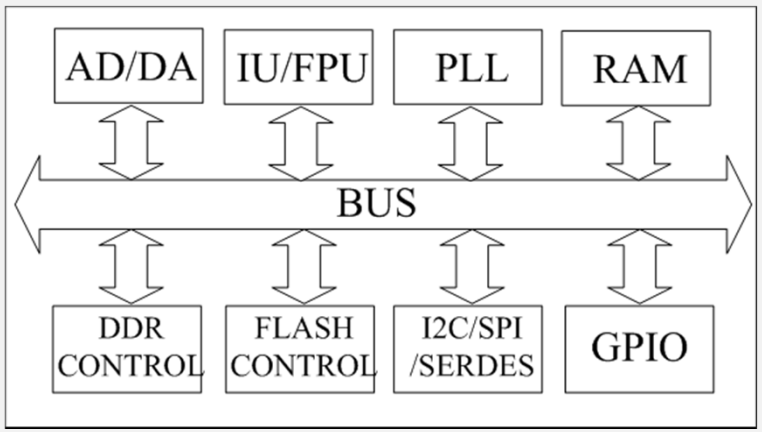
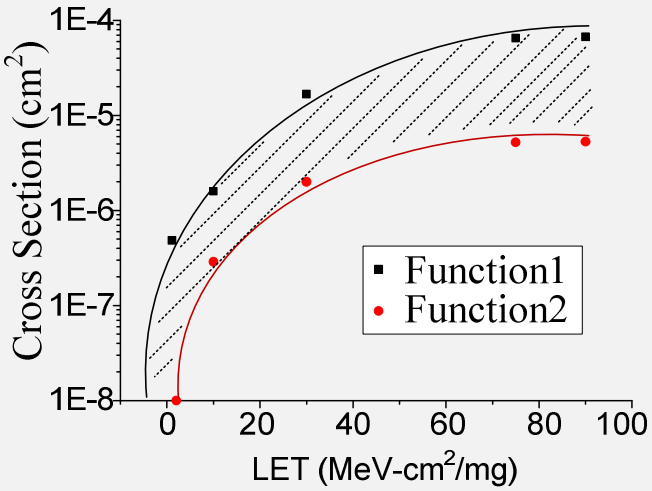
Problem with SEE testing of complex ICs



A typical complex IC

- ✓Many modules
- ✓many function modes

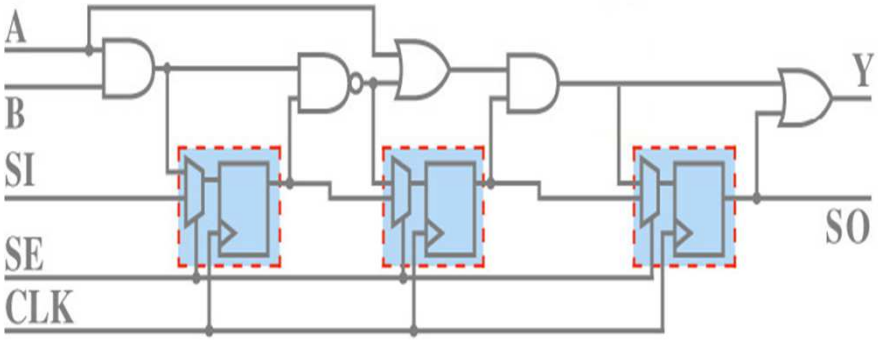


Different cross sections for different function

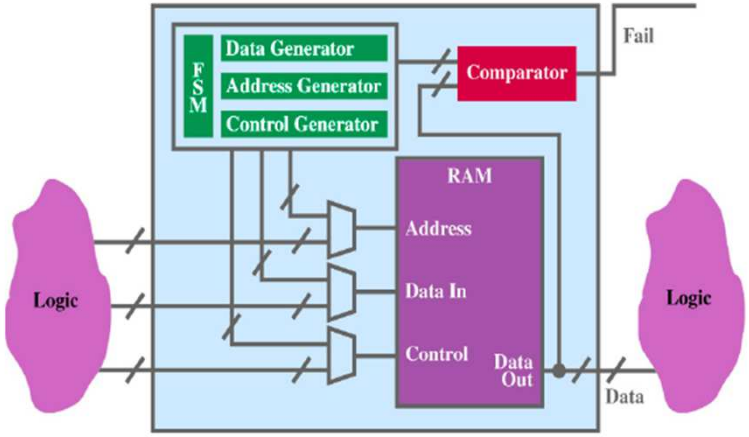
- ➢ **It is very difficult to evaluate and define the SEE hardness of a complex IC by limited function tests**
- ➢ **A simple method which can implement a worst-case test is needed**

SEE testing based on built-in self-test (BIST)

- Built-in self-test (BIST) is a popular and even mandatory design-for-test (DFT) method in nowaday IC designs
- Two of BIST features, Scan chains and Memory BIST (MBIST) can be used for evaluating SEE performance of ICs



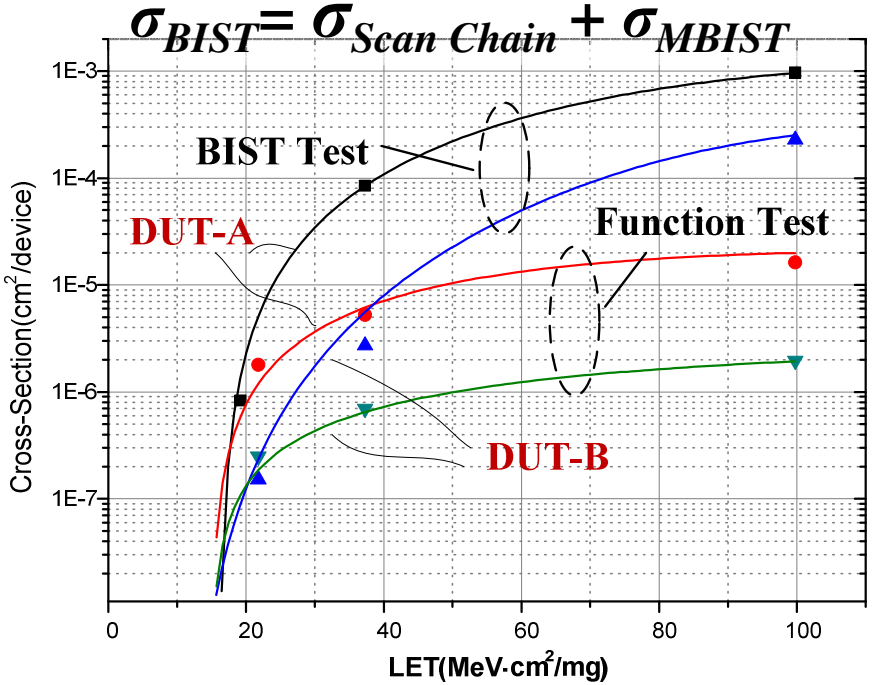
Scan Chain



MBIST

- Almost 100% of sensitive modules in ICs can be covered by BIST test

Comparison between Function and BIST SEE test



Item / Device	LET Threshold (MeV*cm²/mg)	Saturation cross section (cm²/device)
DUT-A BIST	13.6-22.2	9E-4
DUT-A Function		1.5E-5
DUT-B BIST		2E-4
DUT-B Function		2E-6

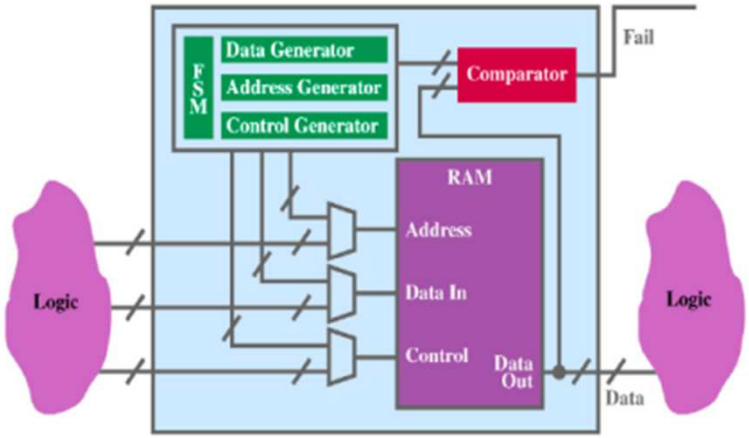
DUT-A and DUT-B are two 0.18μm rad-hard ICs

- σ_{BIST} is always greater than $\sigma_{Function}$
- SEE test with BIST is a worst-case test

BIST test result can be a conservative estimation of any function test results

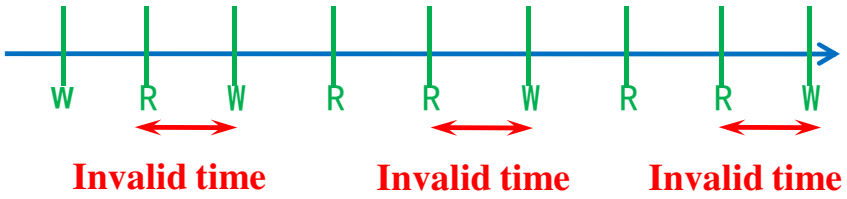
Effective fluence in SEE test with MBIST

Memory BIST



March-2 arithmetic：

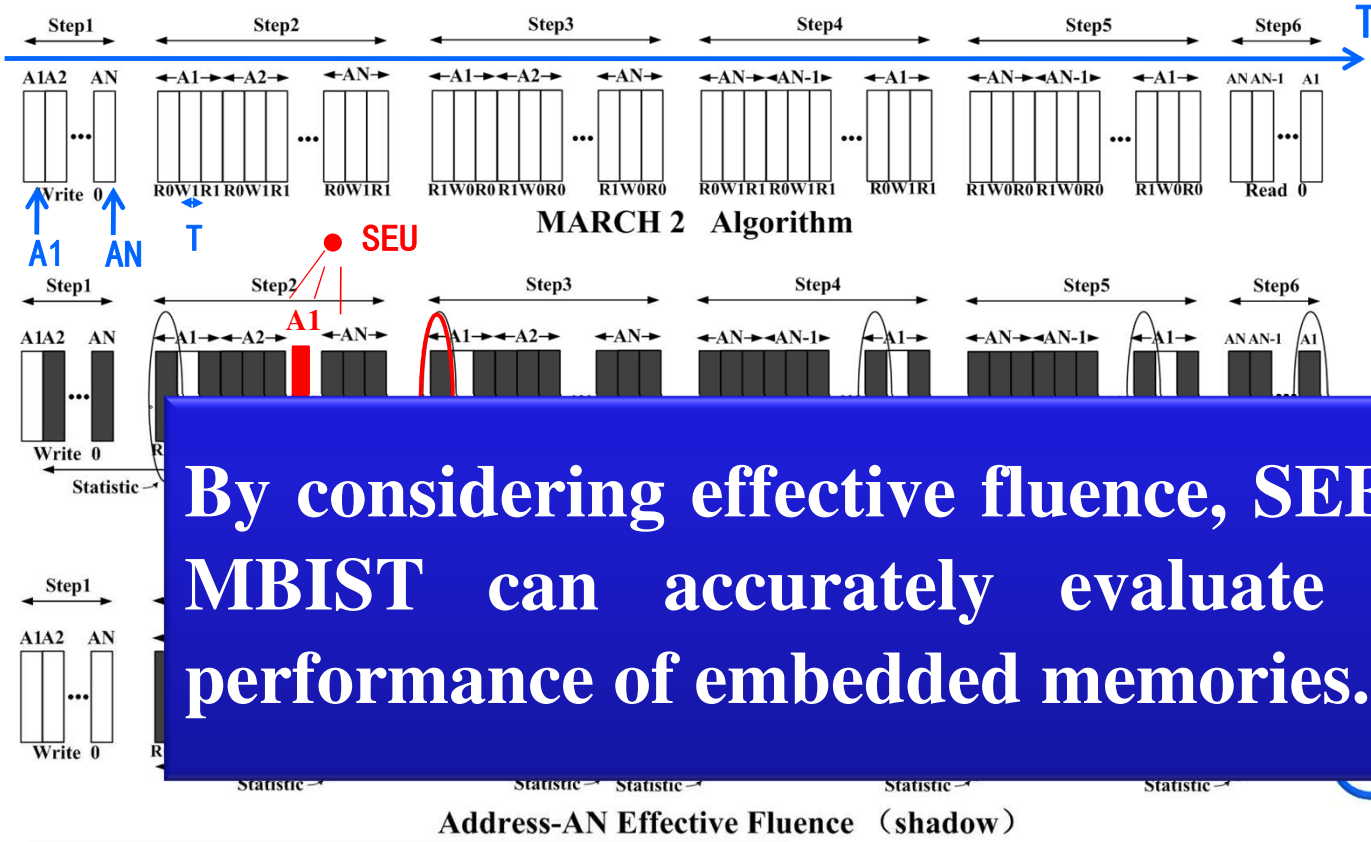
1up	- write 0
2up	- read 0，write 1，read 1
3up	- read 1，write 0，read 0
4down	- read 0，write 1，read 1
5down	- read 1，write 0，read 0
6down	- read 0



- The sequence and timing of MBIST operation is determined by embedded arithmetic, but can't be adjusted
- Not all SEUs can be detected due to self refresh by write operation

Effective fluence should be calculated according to the MBIST arithmetic

Effective fluence in SEE test with MBIST



By considering effective fluence, SEE test with MBIST can accurately evaluate the SEU performance of embedded memories.

The W/R execution sequence of each addr(A1-AN)

Example: A1 and AN SEU Capture Process

ve Time

c Time

$$\frac{14}{14}$$

$$\text{T-5} \approx \frac{12}{14}$$

March-2 arithmetic：

Step 1: up - write 0
Step 2: up - read 0，write 1，read 1
Step 3: up - read 1，write 0，read 0
Step 4: down - read 0，write 1，read 1
Step 5: down - read 1，write 0，read 0
Step 6: down - read 0

$$\text{Efficiency Factor(EF)} = \frac{T_{eff}}{T_{total}} = \frac{13}{14}$$

$$\text{Effective Fluence} = \text{Actual Flucence} \times \text{EF}$$

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Using laser for SEE test

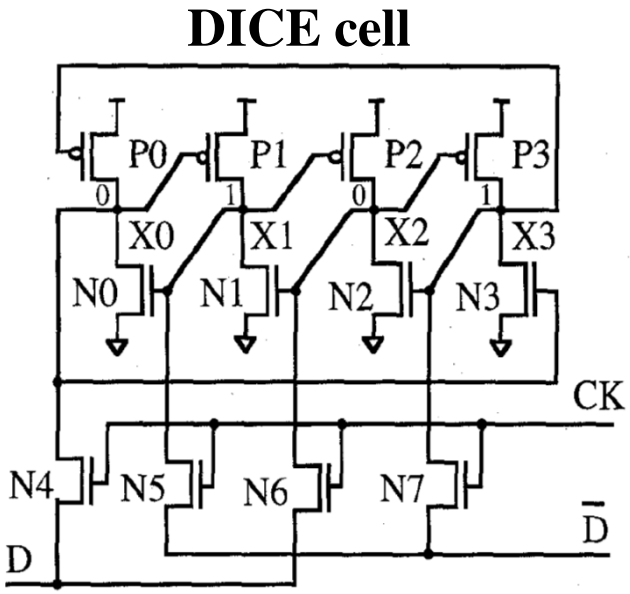
- **Pulsed laser is a good tool to estimate SEE performance of ICs**

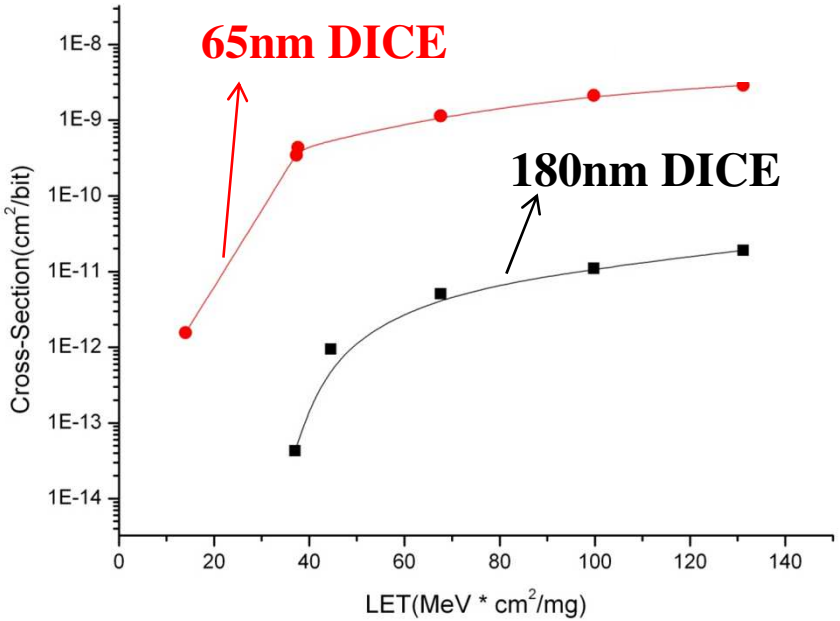
- **In BMTI, we mainly take advantage of laser for:**

  Positioning of SEE errors/failures

Positioning of SEE errors/failures

① Positioning of SEU Sensitive Node in an SEU-hardened SRAM



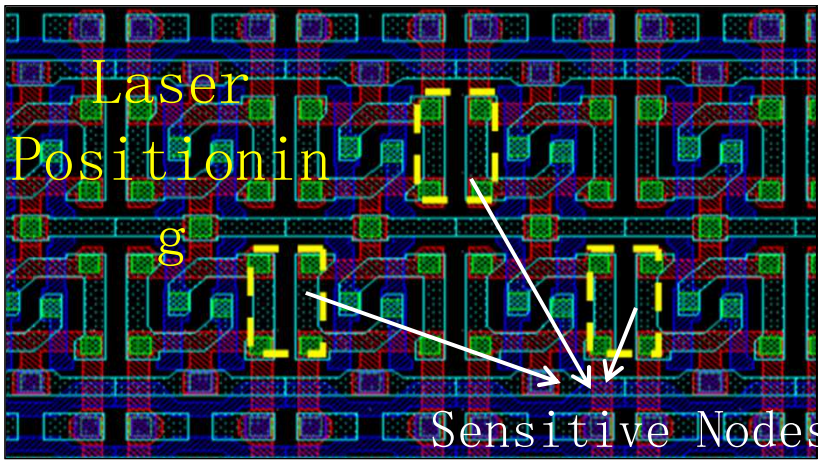


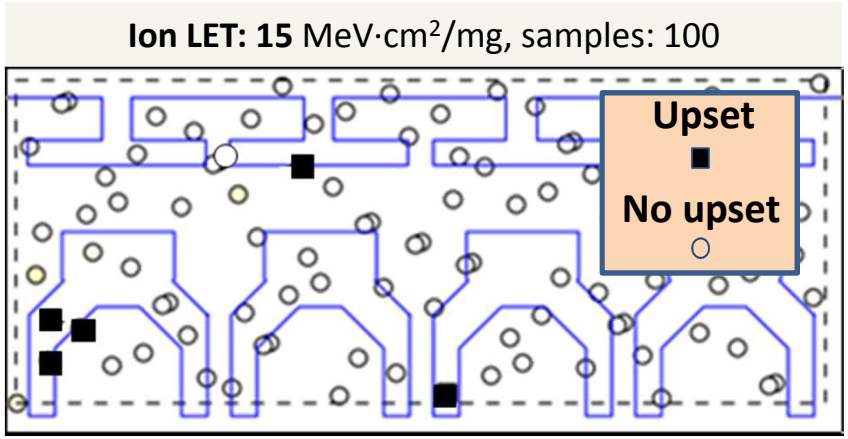
Heavy ion test shows:

- **For a 0.18μm conventional DICE, LET_{th}≈37 MeV·cm²/mg**
- **For a 65nm conventional DICE, LET_{th}<14 MeV·cm²/mg**

Positioning of SEE errors/failures

① Positioning of SEU Sensitive Node in an SEU-hardened SRAM





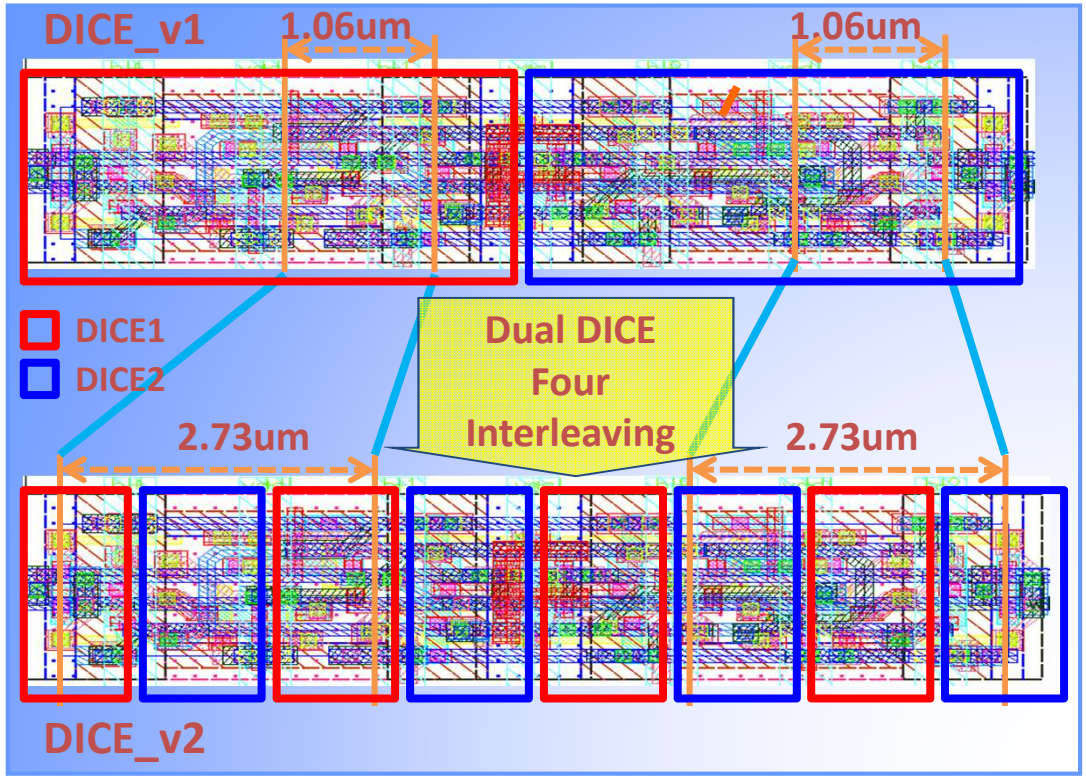
Three areas in a bit cell susceptible to SEUs were found by laser testing.

According to the laser result, TCAD simulation gives the reasons for the sensitivity:

a) **Charge sharing between NMOS**
b) **Charge sharing between NMOS and PMOS, and the bipolar amplification of the PMOS**

Positioning of SEE errors/failures

① Positioning of SEU Sensitive Node in an SEU-hardened SRAM



According to laser and simulation analysis, the SRAM was redesigned by modifying its bit cell:

-Spacing between sensitive nodes increases by 2.7x in an area-efficient manner

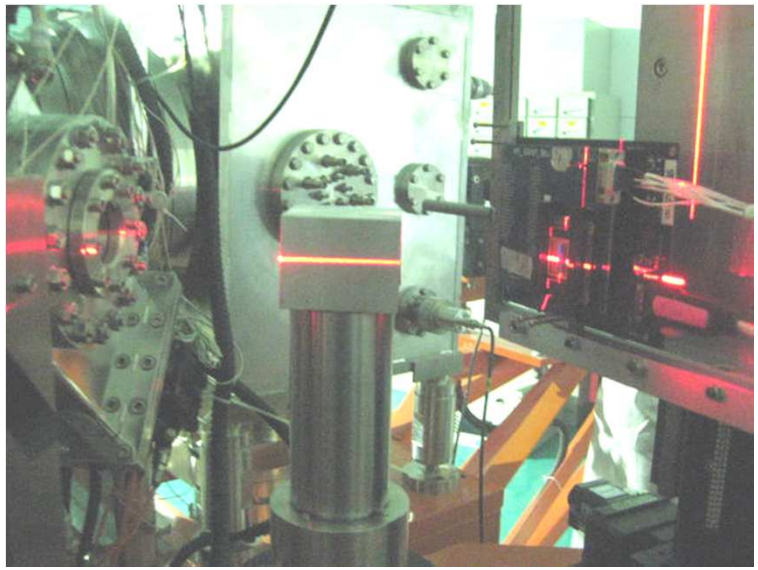
-Negligible cost of power and performance

Heavy ion test shows that the SEU threshold LET of the new SRAM is greater than 37 MeV·cm^2/mg

Positioning of SEE errors/failures

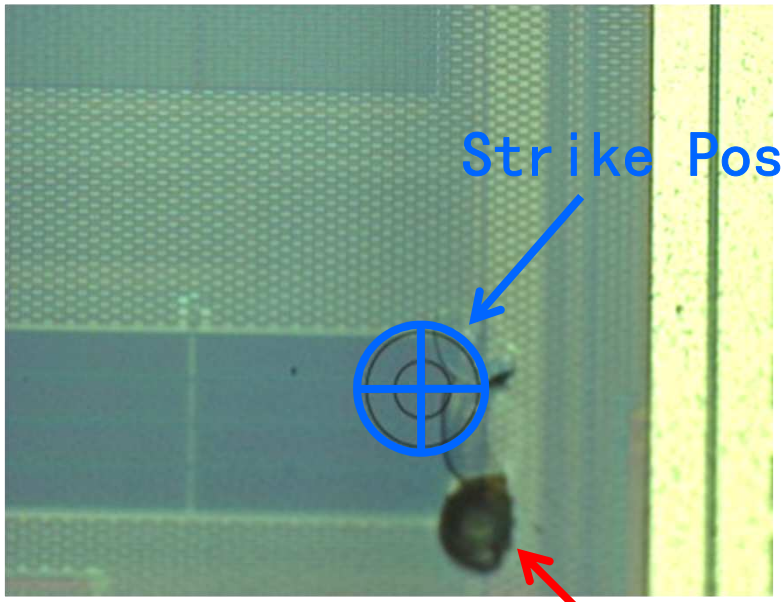
② Failure Analyzing of SEE-induced Burnout

An ADC was burned out under heavy ion irradiation



HIRFL-Accelerator Bi
（LET=93 MeV·cm^2/mg）

Microscopy shows that:
ESD transistor and the inter-connection around it was burned



Positioning of SEE errors/failures

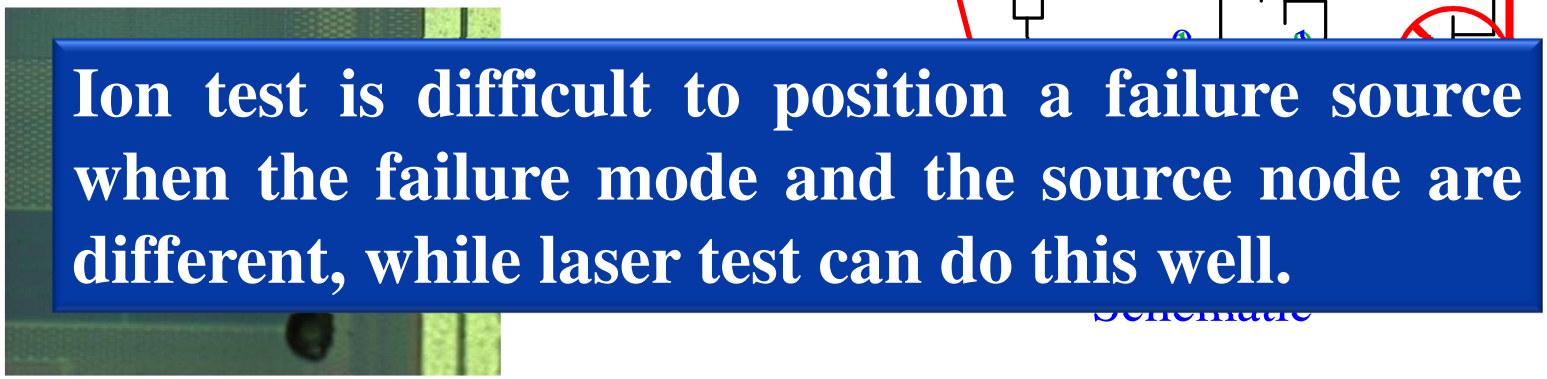
② Failure Analyzing of SEE-induced Burnout

Laser test shows that:

- Direct strike on the ESD transistor doesn't induce burn-out
- Burn-out was found after the strike on the capacitor in the ESD structure

Mechanism Analysis:

The capacitor in the ESD structure can be broken down by irradiation, leading to large current and then burnout



Ion test is difficult to position a failure source when the failure mode and the source node are different, while laser test can do this well.

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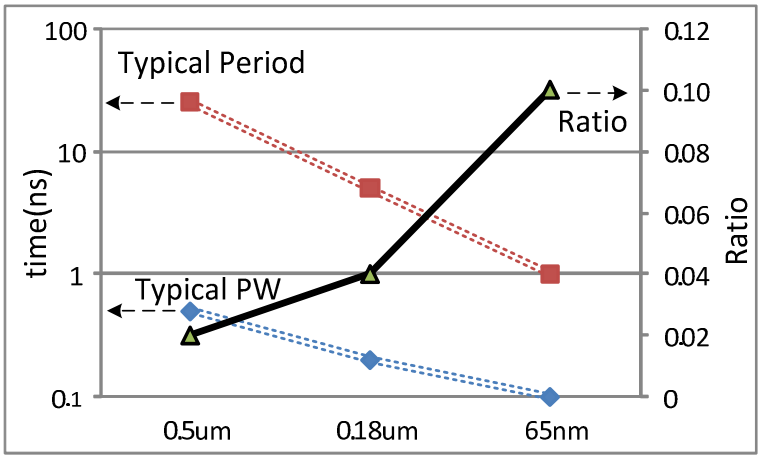
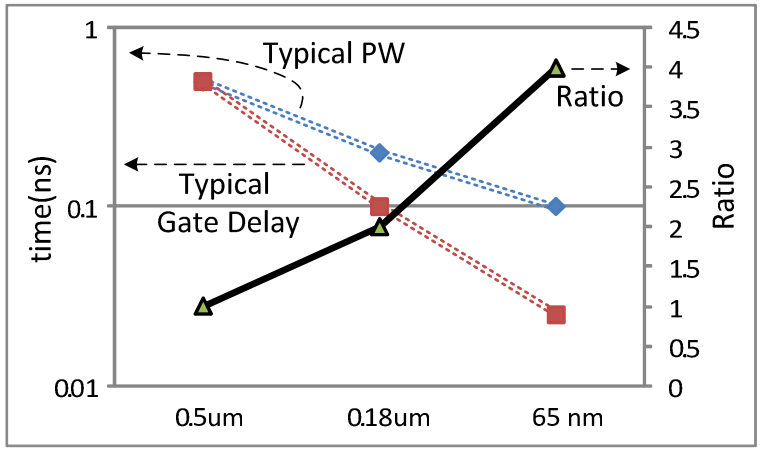
SET has become a serious problem

Pulse Width vs. Period

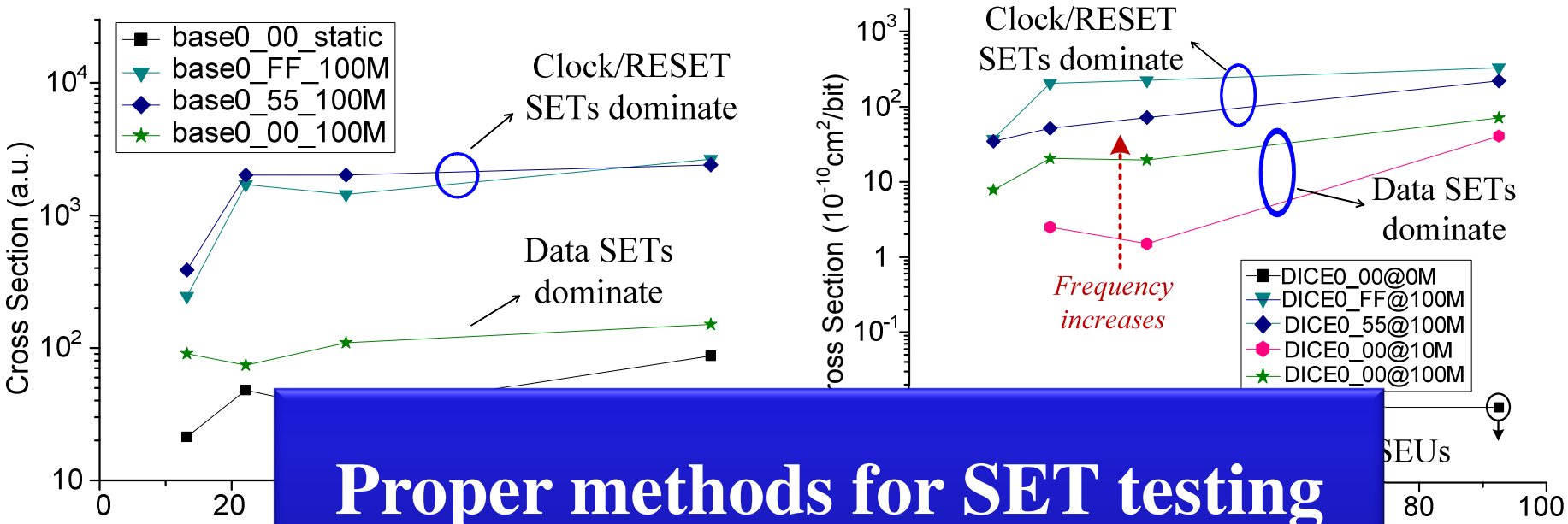


Pulse Width vs. Gate Delay



- As process technology advances, the ratio of typical SET pulse width (PW) and typical circuit period increases, making SETs easier to be captured by sequential cells
- The ratio of typical SET PW and typical cell delay increases, making SETs easier to propagate on logic paths

65nm Test Results – SET vs. SEU



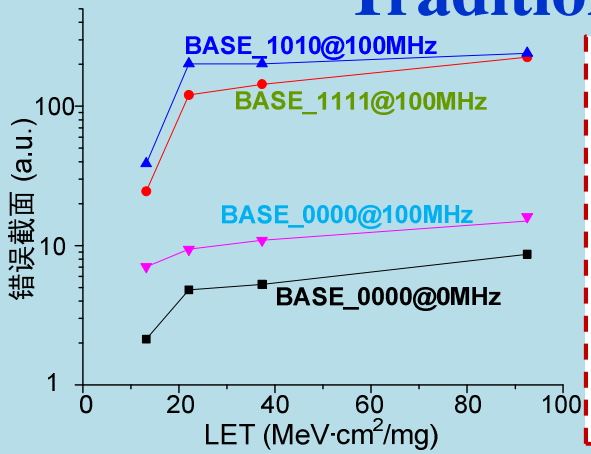
Proper methods for SET testing are necessary for advanced ICs!

An un F chain

- **For a 65nm unhardened circuit, SET surpasses SEU, and becomes the dominate error source**
- **For a 65nm hardened circuit, SET is almost the only error source**

Method for distinguishing SEU and SET

Traditional SEE Test and Analysis Method



①Record total errors after a certain fluence irradiation
②Cross Section = Errors/ Fluence
③Plot Cross Section with LET

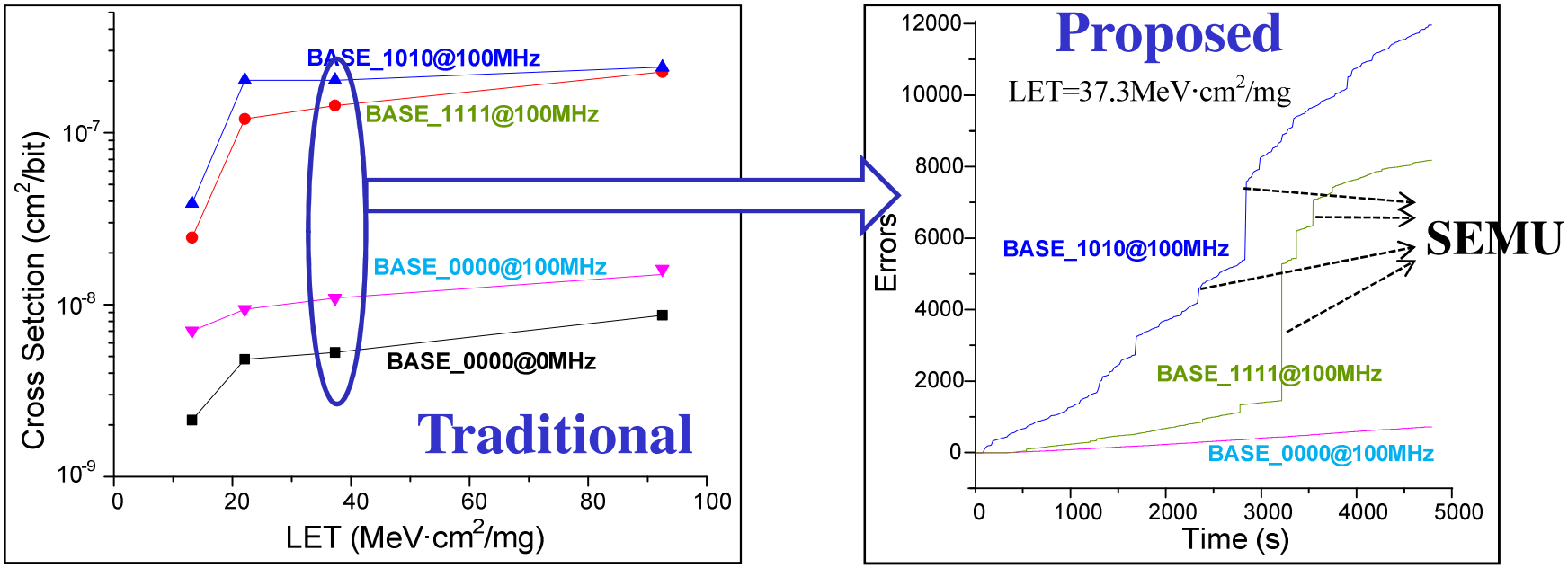
Problem:

- ✓Unable to see how errors accumulate
- ✓Unable to distinguish SEU and SET

Time domain test and analysis

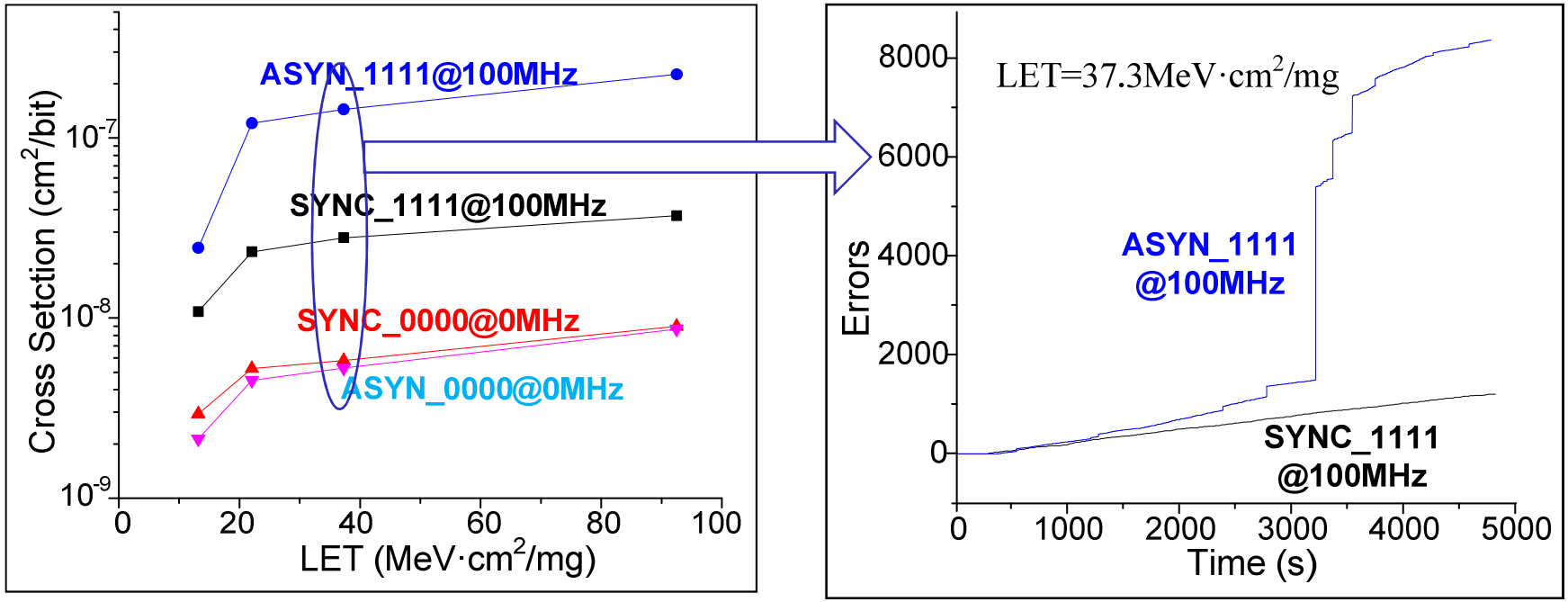
- ➢Record errors every Δt during irradiation
- ➢Δt≤0.1s to make sure only one event happens during Δt
- ➢Plot error accumulation with time for each type of ions
- ➢SEU and SET can be distinguished by observing time-domain plot

Method for distinguishing SEU and SET



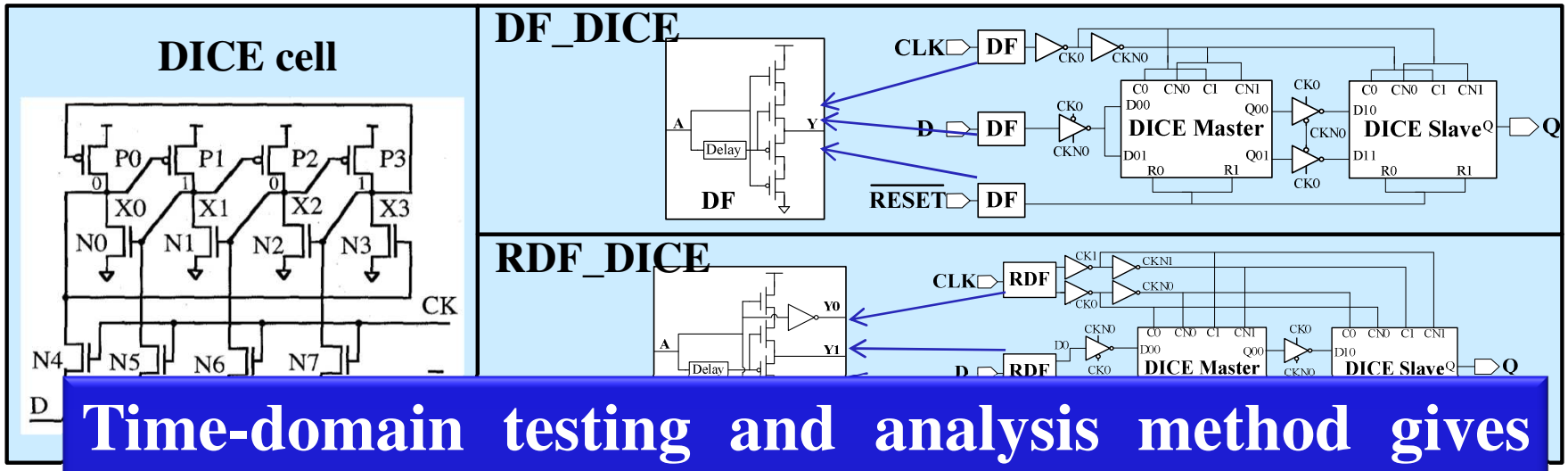
- Plotting errors in time domain provides insight to the detailed process of error accumulation
- Discrete jumps in the time-domain curves indicate single-event multiple-cell upsets (SEMU)
- Single events on global signals such as clock and reset can cause SEMUs (as large as several thousand upsets)

65nm SET– sync reset vs. async reset

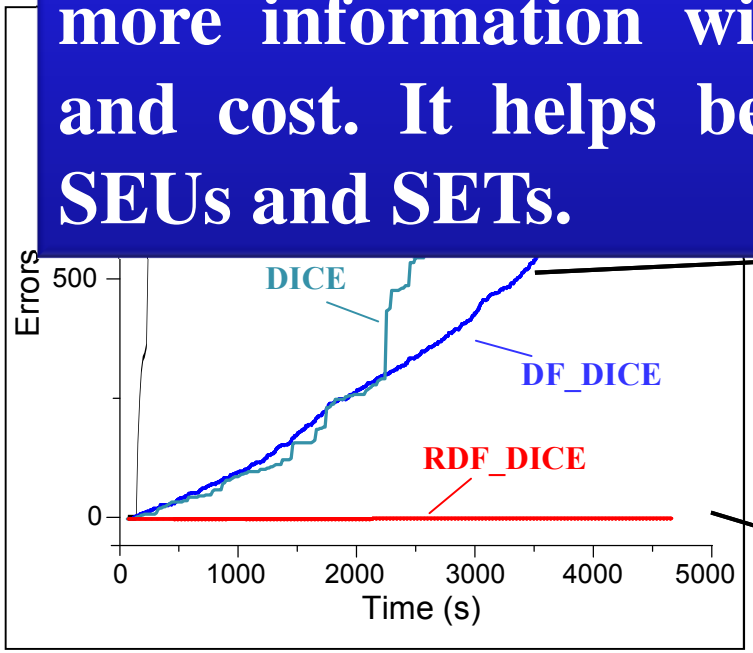


- **Many SET-induced SEMUs happened in the test structure with asynchronous reset**
- **No SEMU was observed in the test structure with synchronous reset**

An application in SEE hardness evaluation



Time-domain testing and analysis method gives more information without additional beam time and cost. It helps better recognize and mitigate SEUs and SETs.



method (delay filter) is useful to mitigate SEMUs but still vulnerable to SETs

Redundant delay filter (RDF) removes SETs completely

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Summary

Radiation assurance test is very interesting, but also very complicated. It always needs joint efforts to find better solutions, and BMTI is looking forward to collaborating with related partners to do this.


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THANK YOU !
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